

Figure 1

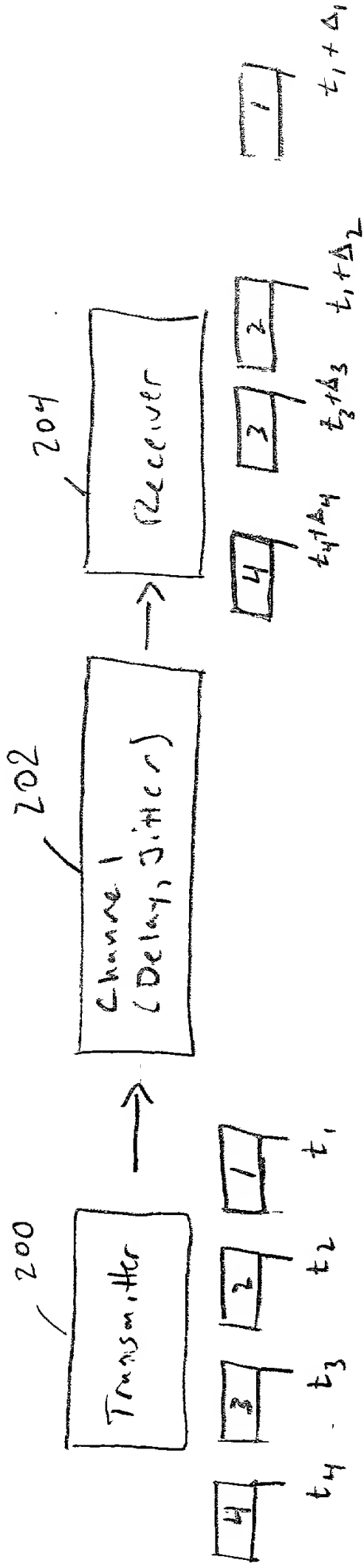


Figure 2

300 ✓

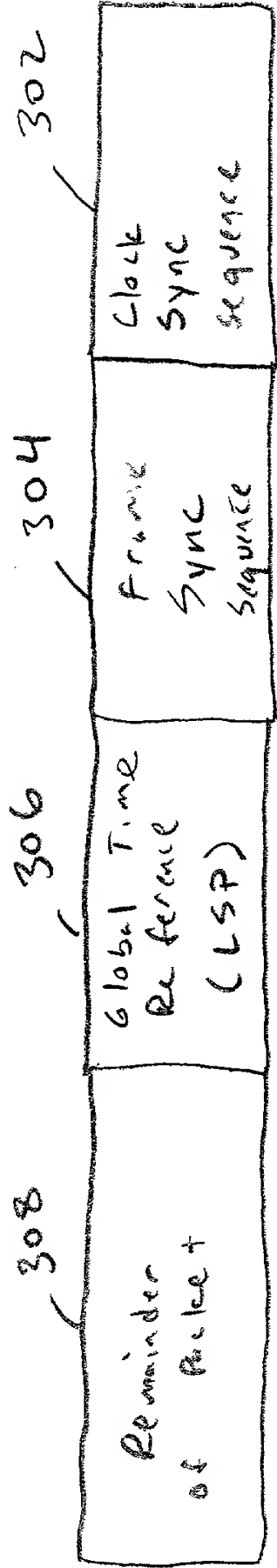


Figure 3

GTR

Figure 4A

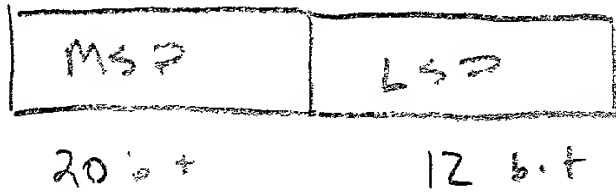
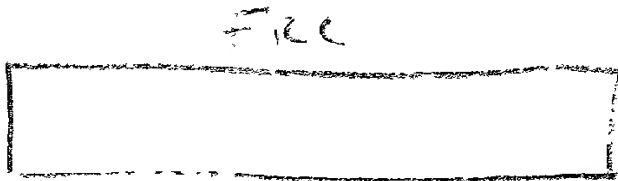


Figure 4B



32 bit

FRCO

Figure 4C

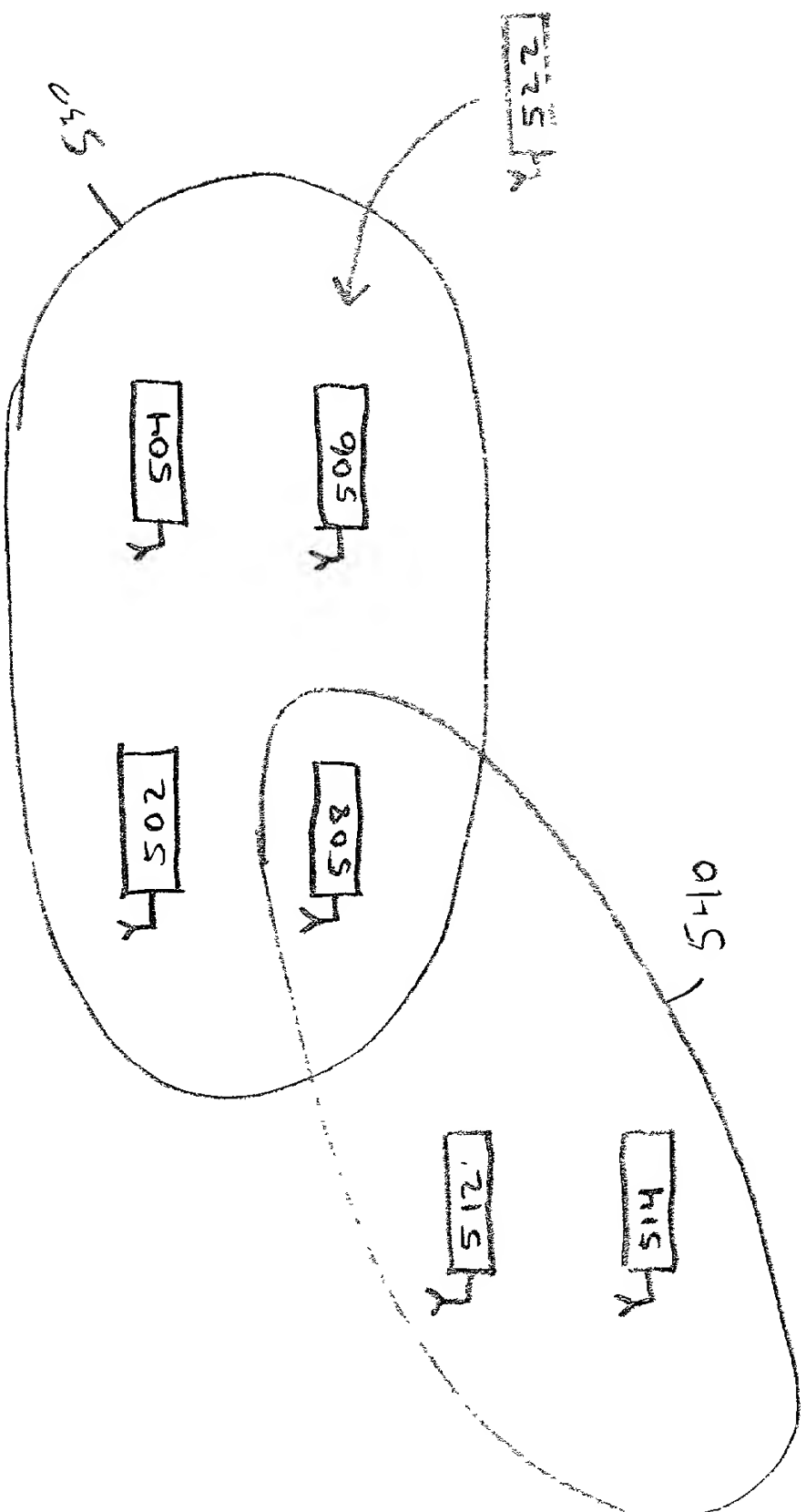


32 bit

$$GTR = FRC + FRCO$$



5 arcs, J



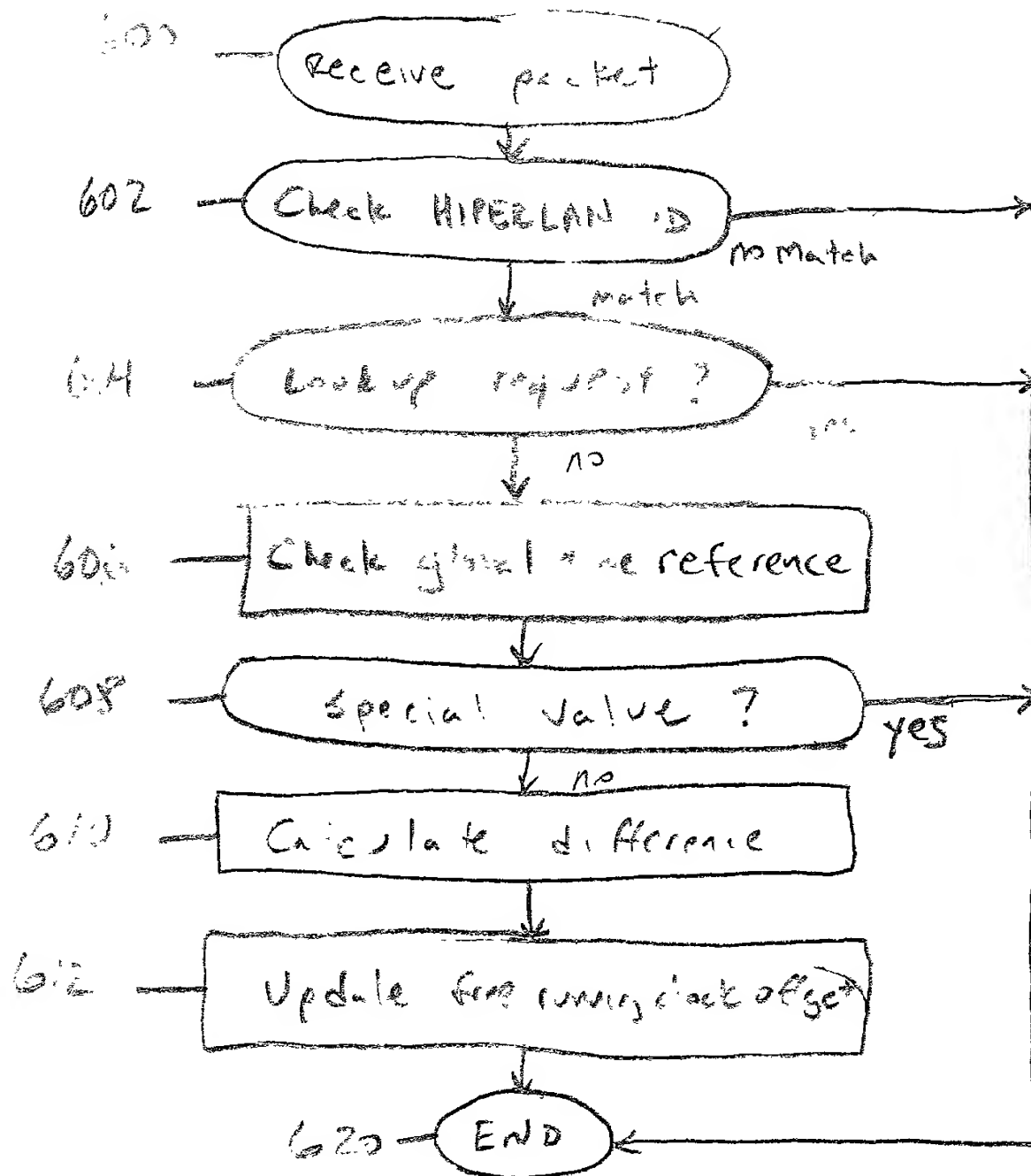


Figure 6

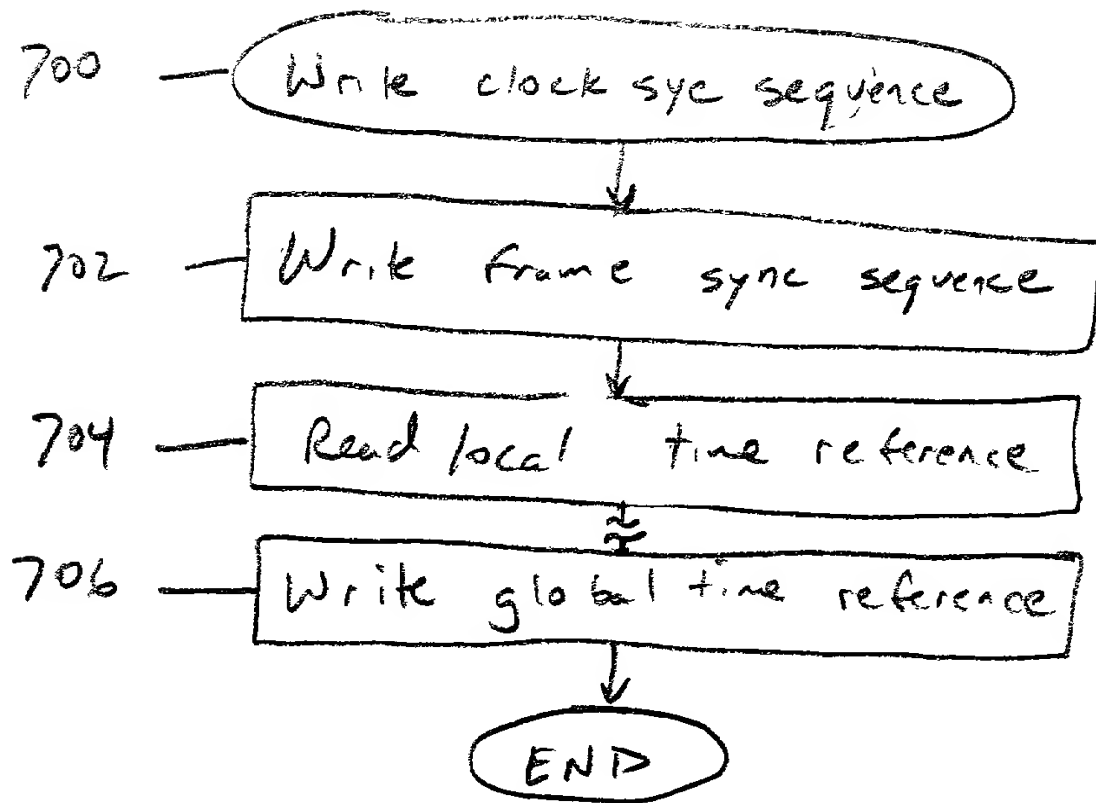


Figure 7A

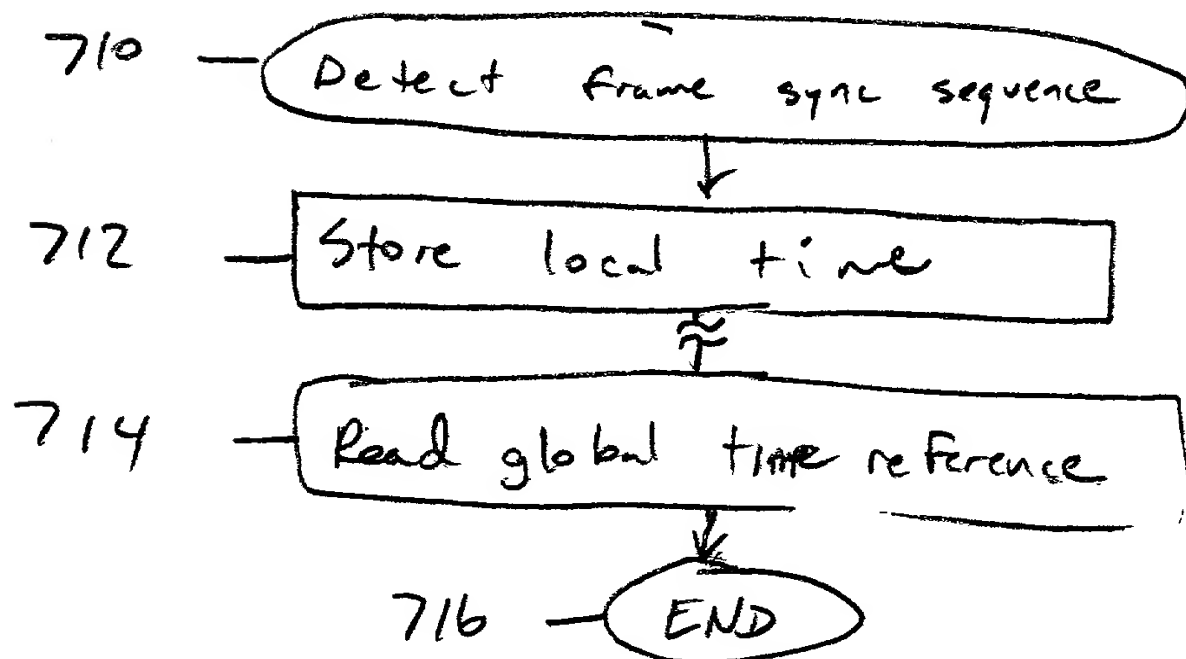


Figure 7B